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10/749,325	12/29/2003	Colin Whitby-Strevens	APPL-P3015	1716

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GAZDZINSKI & ASSOCIATES, P.C.
11440 WEST BERNARDO COURT
SUITE 375
SAN DIEGO, CA 92127

EXAMINER	
SPITTLE, MATTHEW D	

ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/749,325	WHITBY-STREVENS ET AL.	
	Examiner	Art Unit	
	MATTHEW D. SPITTLE	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11,13,15-24,29 and 33-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *29 and 33-42* is/are allowed.

6)☒ Claim(s) *1,3-11,13 and 15-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 42 have been examined.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 13 recite, "...allowing the 10-bit symbol to be removed..." It's unclear what Applicant's intended metes and bounds of the claim are, since the claim appears to cover anything and everything that does not prohibit these actions from occurring.

Claims 3 – 9 and 15 – 21 inherit the indefiniteness of their parent claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stone et al. in view of Crutchfield et al., Tatum et al., Thayer et al., and further in view of Anderson et al.

Regarding claim 10, Stone et al. teach a method of transmitting data across a high-speed serial bus, the method comprising:

Receiving an 8-bit byte (paragraph 42; Figure 5, item 122; Examiner notes that the symbol would have to be an 8-bit byte since the IEEE 802.3-compliant PHY only supports 8-bit data transfers);

Stone et al. fails to explicitly teach the steps of loading and unloading data from the FIFOs in accordance with a first clock and a second clock. Examiner notes that the IEEE 802.3 and IEEE 1394 busses transfer data at different rates, and thus require the data to be transferred into and removed from the FIFOs (Figure 5, 136, 138, 140, 126, 128) at different clock rates. Thus this limitation is inherently present in the system of Stone et al.

If the received 8-bit byte contains a null symbol, then deleting the null symbol (Examiner takes official notice that it is old, and well known in the art to remove data

padding upon receiving a piece of data for processing. White et al. evidence this in column 2, lines 16 – 20, column 4, lines 1 – 4, and Figure 6.

Else, storing the 8-bit byte in a register (Examiner takes official notice that a FIFO may be implemented using registers, as evidenced by Kohn in column 7, lines 8 – 10)

Receiving a second 8-bit byte that does not contain a null symbol and storing the second 8-bit byte in a second register (Examiner takes official notice that a FIFO may be implemented using multiple registers, as evidenced by Kohn in column 7, lines 8 – 10);

Stone et al. teach a FIFO (Figure 5, 136, 138, 140, 126, 128) but fail to teach assembling a 10-bit symbol from the 8-bit byte stored in the first register and appending two bits from the 8-bit byte stored in the second register.

Thayer et al. teach a method of data alignment when transferring data between devices of differing widths for the purpose of improving performance (column 1, lines 12 – 16; column 2, lines 10 – 19; Figures 11A – 11G). Examiner notes that while Thayer et al. does not expressly teach deriving assembling a 10-bit symbol from an 8-bit byte stored in a first register and 2 bits in a second register, they do show, for example, how two a 24-bit symbol can be assembled from 3 8-bit symbols (Figure 11D). Examiner notes that these figures (Figures 11A – 11G) would provide sufficient teaching for one of ordinary skill in this art to develop other permutations of the same method.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the data alignment as taught by Thayer et

al. into the method of Stone et al. and Crutchfield et al. for the purpose of improving performance.

Stone et al. teach placing the symbol in a FIFO, removing the 10-bit symbol from the first FIFO (Examiner notes that, consistent with the operation of a FIFO, in order for the data to move from Figure 5, item 126, to 132, as indicated by the arrows, the symbol would have to be removed from the FIFO) and sending the decoded 10-bit symbol to an IEEE 1394 compliant PHY (Figure 5, item 120).

Stone et al. fail to teach flagged decoding on the assembled 10-bit symbol.

Crutchfield et al. teach receiving a 10-bit signal on an IEEE 1394 bus, and performing 8B10B and control decoding it for the purpose of reducing radiated emissions, and providing DC balance and clock recovery (paragraphs 12, 13). These advantages help to make the method of transmitting data across a high-speed serial bus more reliable.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the method of sending a 10-bit signal as taught by Crutchfield et al. into the method of Stone et al. for the purpose of making the method of transmitting data across a high-speed serial bus more reliable.

Stone et al. fail to teach the IEEE 802.3-compliant PHY having a GMII interface.

Tatum et al. teach using a GMII interface for the purpose of providing high speed data transfer with low cost of implementation and maintenance, in addition to being compatible with previous Ethernet standards (column 2, lines 6 – 26).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate a GMII interface as taught by Tatum et al. into the apparatus of Stone et al. for purpose of providing high speed data transfer with low cost of implementation and maintenance, in addition to being compatible with previous Ethernet standards. This would have been obvious to improve the performance of the system.

Stone et al, Crutchfield et al., and Thayer et al. fail to teach placing the decoded 10-bit signal into a second FIFO in accordance with a third clock, removing the decoded 10-bit symbol from the second FIFO and sending the decoded 10-bit symbol to an IEEE 1394-compliant PHY.

Anderson et al. teach placing the symbol in a second FIFO (Figure 1, item 5);
In accordance with a third clock (column 7, lines 64 – 66):
Removing the decoded symbol from the second FIFO (column 9, lines 13 – 15);
Sending the decoded symbol to an IEEE 1394-compliant PHY (Figure 1, item 2).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the method of Anderson et al. into the method of Stone et al, Crutchfield et al., and Thayer et al. for the purpose of maximizing the opportunity to successfully transmit useful information within an allocated time (column 6, lines 38 – 41. This would have been obvious in order to improve the performance of the system.

* * *

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stone et al. in view of Crutchfield et al., in view of Thayer et al., in view of Anderson et al., and further in view of Voit.

Regarding claim 11, Stone et al., Crutchfield et al., Thayer et al., and Anderson et al. fail to teach wherein the second clock is phase locked to the third clock.

Voit teaches phase locking different clock signals together in order to reduce setup and hold times associated with the components (column 5, lines 45 – 65).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to phase lock, as taught by Voit, the second and third clocks of Stone et al., Crutchfield et al., Thayer et al., and Anderson et al., for the purpose of reducing setup and hold times within the system, thereby improving system performance.

* * *

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stone et al. in view of Crutchfield et al., and further in view of Thayer et al.

Regarding claim 22, Stone et al. teach a method of transmitting data across a high-speed serial bus, the method comprising:

Receiving an 8-bit byte on an IEEE 802.3-compliant PHY (Figure 5, item 122; Examiner notes that the symbol would have to be an 8-bit byte since the IEEE 802.3-compliant PHY only supports 8-bit data transfers);

Stone et al. fails to explicitly teach the steps of loading and unloading data from the FIFOs in accordance with a first clock and a second clock. Examiner notes that the IEEE 802.3 and IEEE 1394 busses transfer data at different rates, and thus require the data to be transferred into and removed from the FIFOs (Figure 5, 136, 138, 140, 126, 128) at different clock rates. Thus this limitation is inherently present in the system of Stone et al.

If the received 8-bit byte contains a null symbol, then deleting the null symbol (Examiner takes official notice that it is old, and well known in the art to remove data padding upon receiving a piece of data for processing. White et al. evidence this in column 2, lines 16 – 20, column 4, lines 1 – 4, and Figure 6.

Storing the 8-bit byte in a register (Examiner takes official notice that a FIFO may be implemented using registers, as evidenced by Kohn in column 7, lines 8 – 10);

Receiving a second 8-bit byte that does not contain a null symbol and storing the second 8-bit byte in a second register (Examiner takes official notice that a FIFO may be implemented using multiple registers, as evidenced by Kohn in column 7, lines 8 – 10);

Stone et al. teach a FIFO (Figure 5, 136, 138, 140, 126) but fail to teach assembling a 10-bit symbol from the 8-bit byte stored in the first register and appending two bits from the 8-bit byte stored in the second register.

Thayer et al. teach a method of data alignment when transferring data between devices of differing widths for the purpose of improving performance (column 1, lines 12 – 16; column 2, lines 10 – 19; Figures 11A – 11G). Examiner notes that while Thayer et al. does not expressly teach deriving assembling a 10-bit symbol from an 8-bit byte stored in a first register and 2 bits in a second register, they do show, for example, how two a 24-bit symbol can be assembled from 3 8-bit symbols (Figure 11D). Examiner notes that these figures (Figures 11A – 11G) would provide sufficient teaching for one of ordinary skill in this art to develop other permutations of the same method.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the data alignment as taught by Thayer et al. into the method of Stone et al. and Crutchfield et al. for the purpose of improving performance.

Stone et al. teach placing the symbol in a FIFO (Figure 5, 136, 138, 140, 126), removing the 10-bit symbol from the first FIFO (Examiner notes that, consistent with the operation of a FIFO, in order for the data to move from Figure 5, item 126, to 132, as indicated by the arrows, the symbol would have to be removed from the FIFO) and sending the decoded 10-bit symbol to an IEEE 1394 compliant PHY (Figure 5, 120).

Stone et al. fail to teach flagged decoding on the assembled 10-bit symbol.

Crutchfield et al. teach receiving a 10-bit signal on an IEEE 1394 bus, and decoding it for the purpose of reducing radiated emissions, and providing DC balance and clock recovery (paragraphs 12, 13). These advantages help to make the method of transmitting data across a high-speed serial bus more reliable.

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the method of sending a 10-bit signal as taught by Crutchfield et al. into the method of Stone et al. for the purpose of making the method of transmitting data across a high-speed serial bus more reliable.

Regarding claim 23, Stone et al. inherently teach wherein a received data valid state is asserted on the IEEE 802.3-compliant PHY since IEEE 802.3 inherently contains a receive data valid state as described in the IEEE 802.3 specification, page 17, section 22.2.2.6.

* * *

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stone et al. in view of Crutchfield et al., Thayer et al. and what is old and well known in this art as evidenced by Smith et al.

Regarding claim 24, Examiner takes official notice that it is old and well known in this art to use a FIFO for speed compensating between two busses of different speeds. Smith et al. evidence this (column 2, lines 45 – 50 teach that speed compensating is done via a padding algorithm. Column 6, lines 23 –24 teach that Figure 6, item 204 is a padding unit. Column 6, lines 37 – 40 teach that Figure 6, item 204 contains a FIFO. Therefore, the FIFO is, at least in part, responsible for the data padding, which is

responsible for speed compensation between the IEEE 802.3-compliant PHY and IEEE 1394-compliant PHY.).

Allowable Subject Matter

Claims 29 and 33 – 42 are allowed.

Claims 1, 3 - 9, 13, and 15 - 21 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Response to Arguments

Applicant's arguments filed 1/14/2008 have been fully considered but they are not persuasive.

Regarding Applicant's argument that Thayer does not teach mapping between a target output which is a non-multiple of the target input, the Examiner notes that Figure 11A shows mapping between a 16-bit input and a 24-bit output, using all 16 bits from a first input, and 8 bits from a second input. This is not unlike the process of mapping between a 10-bit output using 8 bits of a first input and 2 bits of a second input. The Examiner agrees that any 24-bit output stream can always be represented by three separate 8-bit sequences, just as one of ordinary skill in this art would understand that any 10-bit output stream can always be represented by five separate 2-bit sequences.

Regarding Applicant's argument that Thayer has not selected any of his mappings based upon the need to accommodate devices operating on different clocks, the Examiner notes that Thayer is not relied upon for this teaching. Rather, Stone is.

225

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

230 A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any 235 extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the 240 examiner should be directed to MATTHEW D. SPITTLE whose telephone number is (571)272-2467. The examiner can normally be reached on Monday - Friday, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/M. D. S./
Examiner, Art Unit 2111

/MARK RINEHART/
Supervisory Patent Examiner, Art Unit 2111